I CLAIM:

1. An arrangement of bump pads for use on a face of a semiconductor die having four edges, comprising:

a plurality of corner regions, each corner region comprising a first plurality of input/output bump pads and a first plurality of power bump pads, said corner regions each adjoining two edges of said die;

a plurality of edge regions comprising a second plurality of input/output bump pads and a second plurality of power bump pads, said edge regions located along the edges of said die and interleaved between said corner regions; and

a core power region comprising a third plurality of power bump pads, said power region centrally located within said edge regions and said corner groups.

2. The arrangement of bump pads of claim 1 wherein said plurality of edge regions comprise a plurality of linearly aligned bump pad arrays, each linearly aligned bump pad array comprising a plurality of input/output bump pads, a ground bump pad, and a voltage bump pad.

3. The arrangement of bump pads of claim 1 wherein said corner region comprises a corner region standard sector, at least one left corner region sector, and at least one top corner region sector.

4. The arrangement of bump pads of claim 1, further comprising a peripheral power bar passing through said corner regions and said edge regions.

5. The arrangement of bump pads of claim 4, further comprising a plurality of power rails traversing said power core and connecting the power bump pads in said power core with said peripheral power bar.

6. The arrangement of bump pads of claim 2, further

comprising a plurality of input/output cells located at the periphery of said corner regions and said edge regions, and a plurality of interconnections between said input/output bump pads of said corner regions and said edge regions and said plurality of input/output cells.

7. The arrangement of bump pads of claim 3, further comprising a corner region edge sector.

8. The arrangement of bump pads of claim 3, wherein:

said standard signal group comprises a plurality of input/output bump pads, a ground bump pad, and a voltage bump pad, and all of said input/output bump pads, ground bump pad, and voltage bump pad are linearly aligned;

each left corner region sector contains a plurality of left sector input/output bump pads, a left sector voltage bump pad, and a left sector ground bump pad, wherein said left sector voltage bump pad and said left sector ground bump pad are no more than two bump pads from the edge of the die surface; and

each top corner region sector contains a plurality of top sector input/output bump pads, a top sector voltage bump pad, and a top sector ground bump pad, wherein said top sector voltage bump pad and said top sector ground bump pad are no more than two bump pads from the edge of the die surface.

9. A corner region arrangement of bump pads for use on a surface of a semiconductor die having four edges, said corner region adjoining two edges of said semiconductor die surface, comprising a standard signal group and at least one corner region sector.

10. The corner region arrangement of Claim 9 wherein said at least one corner region sector comprises at least one pair of matched corner region sectors.

11. The corner region arrangement of Claim 10 further

comprising a remaining sector.

12. The corner region arrangement of Claim 9 wherein said bump pads comprise a plurality of power bump pads and a plurality of I/O pads, wherein said power bump pads are within two bump pads of an edge of the die surface.

13. An arrangement of bumps for use on a flip-chip die, comprising:

at least one power bump;

a linearly aligned plurality of I/O bumps, wherein said linearly aligned I/O bumps are aligned with each power bump.

14. The arrangement of bumps of Claim 13, wherein each power bump is linearly aligned with and intermediate said linearly aligned I/O bumps.

15. The arrangement of bumps of Claim 14, wherein said ground and power bump and I/O bumps form an array, and said array is replicated linearly across the die surface, thereby forming a linear bump array arrangement.

16. The arrangement of bumps of Claim 15, further comprising a plurality of linear array bump arrangements interspersed with a plurality of linearly aligned core power bumps.

17. The arrangement of bumps of Claim 13, wherein every power bump is located at a single end of said I/O bumps.

18. The arrangement of bumps of Claim 13, further comprising:

a plurality of connections between said I/O bumps and a plurality of I/O cells;

a power ring; and

connections between said power and ground bumps and said

power ring.

19. The arrangement of bumps of Claim 13, comprising a connection between a first I/O bump located furthest from said power and ground bumps emanates in a first direction and a connection between an I/O bump neighboring said first I/O bump and proximately closer to said power and ground bumps emanates in a second direction.

20. The arrangement of bumps of Claim 19, wherein said first direction is opposite said second direction.

21. The arrangement of bumps of Claim 19, wherein connections from said I/O bumps to said I/O cells are approximately equal in length, thereby providing balance in I/O connections.

22. A method for distributing connection pads on a surface of a semiconductor die, said method comprising the steps of:

calculating a power-signal ratio;

establishing a number N of I/O cells to be allocated per power cell group;

arranging the N I/O cells and power cell groups linearly and repeating said linear arrangement within four edge groups on the surface of the die;

allocating four corner regions, one corner region in each corner of the die surface;

arranging a core power group within the center of said edge groups and said corner regions.

23. A method for designing a corner region arrangement of a plurality of I/O bump pads and power bump pads on a die having four edges, comprising the steps of:

establishing a corner region size based on the ratio of I/O bump pads to power bump pads;

designating a first bump pad row;

setting a counter M to one;

designing an M+1 sector by designating as many bump pads as may be located within the leftmost column to belong to the M+1 sector;

designing an M+2 sector by designating as many bump pads as may be located within the topmost row to belong to the M+2 sector;

filling the remainder of the M+1 sector by designating bump pads within the top of the leftmost remaining column to belong to the sector;

filling the remainder of the M+2 sector by designating bump pads on the left of the topmost remaining row to belong to the sector;

evaluating whether the sector is complete, and if the sector is incomplete, repeating said M+1 filling step and said M+2 filling step until the sector is complete;

incrementing the counter to M+2;

deciding whether more than one sector remains, and repeating said M+1 sector design step and all subsequent steps when one more than one sector remains until one or less sectors remain; and

determining whether one sector remains and if one sector remains designating all remaining undesignated bumps to the final sector.

24. The method of Claim 23 further comprising the step of designating two bump pads in each sector closest to an edge of the die as power bump pads, wherein said two bump pad designating step is subsequent to said one sector remaining determining step.

25. The method of Claim 24 further comprising the step of providing balanced connections between said bump pads and a power ring and a plurality of I/O cells located near the edge of said die.